# Faculty Personal Information

**Mr.A.RAJESH**

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|---|---|---|
| **Designation** | : | Assoc Professor |
| **Years of Experience** | : | 13 Yrs |
| **Email Id** | : | rajeshakula07@gmail.com |
| **Employment Status** | : | Full Time - Ratified by JNTUH |
| **Areas of Research** | : | Low Power VLSI |
| **UG Degree** | : | B. Tech (Electronics and Communication Engineering) |
| **PG Degree** | : | M. Tech(VLSI SYSTEM DESIGN) |
| **Ph.D** | : | Pursuing |

**Subjects Taught:**

1. Probability theory and Stochastic Process
2. Signals & Systems
3. Electronic Devices & Circuits
4. Switching Theory & Logic Design
5. Digital Design using Verilog HDL
6. Electromagnetic waves & Transmission Lines
7. VLSI Design
8. Electronic Measurements Instrumentation
9. Telecommunication & Switching Systems
10. Television Engineering
11. Embedded systems Design
12. Algorithms for VLSI DesignAutomation(M.Tech)
13. Digital System Design(M.Tech)
14. VLSI Technology & Design(M.Tech)

**Academic Achievement**: Worked as Incharge HOD, Exam Branch Incharge, M.Tech

Coordinator,90% Pass Percentage for subjects EMTL,S&S,ESD.

**No. of publications in International journals: 08**

1" **Reduction of Power Dissipation & Parameter Variations in VLSI Circuits for SOC"** International Journal of Review in Electronics & communication Engineering(**IJRECE**),Vol.2,No.3,ISSN No:-2321-3159,pp.111-117,June 2014.

2." **Low Power Multi GHz Circuit Techniques in VLSI",** International Journal of Electronics & Communication**(IIJEC**), Vol.3,No.3,ISSN No:-2321-5984,pp.1-7,March 2015

3. "**Clock Distribution using Multiple Voltages",** International Journal of Innovative Research in Advanced Engineering(**IJIRAE**)," Vol.2,No.5,ISSN No:-2349-2163,pp.181-187,May 2015

4. "**Dual -VDD,Single Frequency Clocking Methodology for System on Chip**", Journal of Emerging Technologies and Innovative Research(**JETIR**), Vol.2,No.6,ISSN No:-2349-5162, pp.1791-1798,June 2015

5. " **A High Performance Clock Distribution Network for System on Chip,"**(**IRJET**), International Research Journal of engineering & Technology," Vol.2,No.3,ISSN No:-2395-0056,pp.1049-1056,June 2015.

6. " **Design and Analysis of High Performance and Low Power Current Mode Logic CMOS,"** International Journal of Research in Signal Processing, Computing & Communication-System Design**(IJSPCS),** Vol.1,No.2,ISSN No:-2395-5187,pp.13-17,Dec 2015.

7. ," **Dual Vdd and Single Vth Level Converter for Clock Distribution Network",** 3rd International Conference on Electrical ,Electronics,Engineering Trends,Communication,Optimization and Sciences, **IET ,** 1-2 June 2016

8. ," **Design of Voltage Controlled Oscillator for Clock Synchronization in Phased Locked Loop**", IOSR Journals of VLSI & Signal Processing(IOSR-JVSP), **,** Vol.6,No.3,ISSN No:-2319-4200**,** pp.66-73,3 July 2016

**No. of publications in International Conferences: 05**

1. " **Design of High Performance Phase Locked Loop for Clock Synchronization**" The Fifth International Conference on Wireless Communications, Vehicular Technology, Information Theory, Aerospace and Electronic Systems**(Wireless Vitae 2015)- Global Wireless Summit (GWS), JNTUH** Dec 13 – 16, 2015.

2. " **Design and Analysis of High Performance and Low Power Current Mode Logic CMOS"** 4th International Conference on Communications, Signal Processing, Computing and Information Technologies**(ICCSPCIT 2015),ISBN No:** 978-93-83038-27-5,pp.281-284, Dec 18-19, 2015.

3. " **Design of Low Power & High Performance Dual Vdd and Multi Vth Level Converter**", Joint International Conference on Artificial Intelligence & Evolutionary Computations in Engineering Systems**(ICAIECES-2016) & (ICPCIT-2016**), **SRM University Chennai,pp. 115-116,**19-21 May 2016.

4. " **Dual Vdd and Single Vth Level Converter for Clock Distribution Network ,"** 3rd International Conference on Elec. ,Electronics,Engg Trends,Commn,Optimization and Sciences,**(EEECOS-2016), ,pp/121-126,** 1-2 June 2016.

5." **Design of Level Converters for Low Power Scheme in Clock distribution Networks. ,"** 3rd International Conference on Elec. ,Electronics,Engg Trends,Commn,Optimization and Sciences.**(EEECOS-2016), ,pp.121-126,** 1-2 June 2016

**No. of publications in National Conferences: 01**

1." **Design of a Differential Amplifier using Current Mirror as Active Load** " Third National Conference on Signal Processing,VLSI and Embedded Systems , **ISBN No:-** 978-93-83459-63-6, pp.129-131,June 2014

**Projects guided:** B.Tech –44, M.Tech- 13

**Memberships in Professional Bodies:**

1. LMISTE

**Additional Responsibilities in the Department**:

1. Lab In-charge (VLSI Lab)
2. Class Incharge
3. Faculty Development Programme Incharge
4. Workshops Incharge
5. Guest Lecture Incharge
6. Anti Ragging Committee Member
7. Proctor for Final Year Students.