# Faculty Personal Information

**Mr.A.RAJESH**

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|---|---|---|
| **Designation** | : | Assoc .Professor |
| **Years of Experience** | : | 17 years |
| **Email Id** | : | a.rajesh@aceec.ac.in |
| **Employment Status** | : | Full Time - Ratified by JNTUH |
| **Areas of Research** | : | Low Power VLSI |
| **UG Degree** | : | B. Tech (Electronics and Communication Engineering) |
| **PG Degree** | : | M. Tech(VLSI SYSTEN DESIGN) |
| **Ph.D** | : | Pursuing(JNTUH) |

**Subjects Taught:**

1. Probability theory and Stochastic Process
2. Switching Theory and Logic Design
3. VLSI Design
4. Electromagnetic waves and Transmission lines
5. Signals and Systems
6. Embedded System Design
7. Electronics Measurement and Instrumentation
8. Electronic Devices & Circuits
9. Digital Design using Verilog HDL
10. Pulse Digital Circuits
11. Microprocessors & Microcontrollers
12. Analog Communication

**No. of publications in International journals:**

1. Paper on**" Design and Implementation of CAN Controller for Embedded systems**" at nternational Conference(ICIECE-2012) to be held on 20-21 July 2012 under Gurunanak Institute of Technology,Hyd.
2. A Paper on "**An Efficient Architecture of Low Power CSLA for Data Processing Applications**" at 2nd INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2013) August 9-10, 2013,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506
3. A Paper on "**Design of blanking interface module (BIM) & duty cycle measurement (DCM) module for external system interface unit for receiver Application**" at 3rd INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2014) July, 18-19, 2014,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506.
4. A Paper on "**Design& implementation of a third generation (3G) mobile communication standard-TDSCDMA"** at 3rd INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2014) July, 18-19, 2014,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506.PP.NO.50
5. A Paper on "**Design& implementation of wideband CDMA (WCDMA)for mobile Communication** " at 3rd INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2014) July, 18-19, 2014,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506.PP.NO.50
6. A Paper on "**Data Encoding Techniques for Reducing Energy Consumption in Network on Chip"** at 4th INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2015) August, 21-22, 2015,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506.
7. A Paper on "**An Optimized Design of Secure Differential Logic Gates for DPA Resistant Circuits**" at 4th INTERNATIONAL CONFERENCE ON INNOVATIONS IN ELECTRONICS & COMMUNICATION ENGINEERING (ICIECE - 2015) August, 21-22, 2015,GNIT, Ibrahimpatnam, R.R. District., Hyderabad, A.P, India Pin-501506.
8. A Paper on "**Design of High Performance Phase Locked Loop for Clock Synchronization**" at THE FIFTH INTERNATIONAL CONFERENCE ON WIRELESS COMMUNICATIONS, VEHICULAR TECHNOLOGY, INFORMATION THEORY, AEROSPACE AND ELECTRONIC

SYSTEMS(Wireless Vitae 2015)**-Global Wireless Summit-2015** at Dec 13 – 16, 2015 at Novotel, HICC, Hyderabad

9. A Paper on "**Design and Analysis of High Performance and Low Power Current Mode Logic CMOS**" at INTERNATIONAL CONFERENCE ON COMMUNICATIONS, SIGNAL PROCESSING, COMPUTING AND INFORMATION TECHNOLOGIES at December 18-19, 2015 at MallaReddy College of Engineering and Technology, Hyd.

11. A Paper on "**Design of Low Power & High Performance Dual Vdd and Multi Vth Level Converter**" Joint International Conference on Artificial Intelligence & Evolutionary Computations in Engineering Systems (ICAIECES-2016) & (ICPCIT-2016) 19-21 May 2016 pg.no.115-116.

12. A Paper on **" Dual Vdd and Single Vth Level Converter for Clock Distribution Network**" at 3rd International Conference on Elec. ,Electronics,Engg Trends,Commn,Optimization and Sciences (EEECOS-2016) 1-2 June 2016.

13. A Paper on "**Design of Level Converters for Low Power Scheme in Clock distribution Networks**" at 3rd International Conference on Elec. ,Electronics,Engg Trends,Commn,Optimization and Sciences (EEECOS-2016) 1-2 June 2016.

**No. of publications in International Conferences:**

**1.** Publish in International Journal on "**VHDL Implementation of Turbo encoder and decoder using Log-Map based Iterative Decoding**" at International Journal of Electronics and Communications (IJEC), Volume – 1, Issue – 1, August 2012 .ISSN 2279 – 0098.

**2.** Published in international Journal **on "Implementation of Turbo Decoder using Soft input soft output Iterative Decoder "** at IJSETR, Vol-3,Issue-13,PP.No.2937-2944,June 2014 ISSN No. 2319-8885.

**3.** Published in international Journal **on "Reduction of Power Dissipation and Parameter Variation in VLSI circuits"** at IJRECE, Vol-2,Issue-3,PP.No.111-117,June 2014 ISSN No. 2321-3159.

**4.** Published in international Journal on **"A High Speed Double Precision Binary Floating Point Multiplier using Dadda Algorithm"** at IJRIS, Vol-3,Issue-9,PP.No.14-25,September 2014 ISSN No. 2319-9725.

**5.** Published in International Journal on "**Low Power Multi GHz Circuit Techniques in VLSI**" at IIJEC,Vol.3 ,Issue-3,PP.No.001-007,March 2015,ISSN No.2321-5984.

**6.** Published in International Journal of Innovative Research in Advanced Engineering on "**Clock Distribution using Multiple Voltages**" at IJIRAE, Vol.3 ,Issue-5,ISSN No.2349-2163.

**7.** Published in International Research Journal of Engineering & Technology on "**A High Performance Clock Distribution Network for System on Chip**" at IRJET, Vol.3 ,Issue-3,ISSN

No.2395-0056

**8.** Published in Journal of Emerging Technologies & Innovative Research on "**Dual-VDD, Single-Frequency Clocking Methodology for System on Chip "** at JETIR, Vol.3 ,Issue-6, ISSN No.2349-5162.

**9.** Published in International Journal of Research in Signal Processing, Computing & Communication-System Design on "**Design and Analysis of High Performance and Low Power Current Mode Logic CMOS**" at **(IJSPCS),**Dec **2015** ISSN No: 2395-5187

**10**. Published in **I J C T A**, 9(15), 2016, © International Science Press on "**Design of LowPower & High Performance Dual Vdd and Multi Vth Level Converter"** 9-21 May **2016** pp. 7479-7488.

11. Published in **COMMUNICATION, NETWORKS AND COMPUTING-2018 on** "**A High Performance BPSK Trans Receiver Using Level Converter for Communication Systems**".**Springer Series** Journal.CNC-2018.

**Workshops/ Faculty Development Programs attended:**

**Workshops Attended:-**

1. Attended a two days workshop on DSP Processors and its Applications held during 17th and 18th february, 2006 at T.K.R College of Engineering and Technology, Hyd..
2. Attended a two days workshop on **CMOS VLSI & ASIC Design** held during 10th and 11th August, 2007 at JNTU College of Engineering & Technology, Hyderabad
3. Attended a four days workshop on **VLSI Design & Testing using Tanner Tools** held during 18th to 21 th February, 2008 at Aurora's Technological Research Institute, Hyd.
4. Attended a two days National workshop on **Embedded Systems Design** held during 04th and 05th August, 2008 at T.K.R College of Engineering and Technology, Hyd.
5. Attended a three days workshop on **Analog & Mixed Signal Design** held during 19th to 21th August, 2009 at JNTU College of Engineering & Technology, Hyderabad.
6. Attended a two day course on Model based design for **Embedded systems** at Hotel Taj Krishna organized by Cranes Software Solutions. India.
7. Attended a two week AICTE Sponsored Faculty Development Programme on **Advanced VLSI Design** at Geetanjali College of Engineering & Technology from 17.06.2013 to 29.06.13.
8. Attended a 5 day Faculty Development Programme on **Instructional Design & Delivery** from 03.12.2013 to 07.12.2013 at ACE Engg College, Ghatkesar.
9. Attended **3rd Research Methodology** Course at JNTU, Hyderabad from 16.12.2013 to

21.12.2013.

10. Attended a Two days National workshop on "**CMOS VLSI & ASIC DESIGN USING CADENCE TOOLS**" on 28th 29th January 2014 at ACE Engg College, Ghatkesar,Hyd.

11.Attended a Four Day workshop on "**Mixed Signal IC Design" at Anurag Group of Institutions** during 28 July to 31 July 2015.

12.Attended a Two day FDP on "**Analog & Digital Circuit Design using Cadence Tools at** MVSR Engg College,Hyd during 12-13 January 2016.

13.Attended a Two Week FDP on "**CMOS Mixed Signal and Radio Frequenc VLSI Design**" during 26.12.2016 to 04.02.2017 at VITS,IITKHP.1

14. 5 Days online STTP"**MATLAB based Teaching-Learning in Mathematics,Science & Engineering**" Ramrao Adik Institute of TEchnology,Navi Mumbai.18th to 22nd May 2020.

15.5 Day Online FDP on "Advanced Python Programming using Django" Malineni Lakshmaiah Women's Engineering College,Guntur21-25th May 2020.

16.5 Day Online FDP on "Innovative Trends in Data Analysis with AI" Malineni Lakshmaiah Women's Engineering College,Guntur 26-30th May 2020

**Workshops Conducted:-**

1. Organized a two day workshop on **Digital Signal Processors and its Applications** held during 17th and 18th February, 2006 at T.K.R College of Engineering and Technology, Hyderabad.
2. Organized a two days National **workshop on Embedded Systems Design** held during 04th and 05th August, 2008 at T.K.R College of Engineering and Technology, Hyderabad.
3. As a Coordinator organized the **National Paper Presentation "Prathibha**" held during the months of February and September in the years 2005, 2006,2007,2008,2009 held at T.K.R College of Engineering and Technology, Hyderabad.
4. Organized a two day workshop on **Latest Advances in Electronics and Communication Systems** on 1st, 2nd March 2013 at TKRCET.
5. Organized a Two days National workshop on **CMOS VLSI & ASIC DESIGN USING CADENCE TOOLS** on 28th ,29th January 2014 at ACE Engg College,Ghatkesar,Hyd.
6. Organized a Two days National workshop on **VLSI DESIGN USING Mentor Graphics** during

October 2019 at ACE Engg College,Ghatkesar,Hyd

**NPTEL CERTIFICATE:**

Attended 12 week FDP on "Digital Electronic Circuits" during JAN-APR 2019.

**Projects guided:**

1. B.Tech – 40
2. M.Tech- 15

**Memberships in Professional Bodies:**

1. LMISTE

**Additional Responsibilities in the Department**:

1. In-charge of First Year.
2. FDP/STTP Coordinator of ECE Dept.
3. NBA Work Criteria 5.
4. Mentor for 3 year 20 students
5. VLSI & ECAD Lab Incharge.
6. Anti Ragging Incharge Coordinator

**Books Published:-**

1. ” **Audio and Video Systems**” for Diploma IV sem ECE under VGS Publishers.
2. ”**Digital Electronics and Microcontrollers**” for Diploma IV sem EEE under VGS Publishers.
3. ” **Microcontrollers**” for Diploma VI sem ECE under VGS Publishers.
4. ”**Digital Electronics and Microcontrollers**” for Diploma V sem EEE under VGS Publishers

**Patent:-** Effective Management Analysis of Signal Coverage and Novel design of Traingular Patch Antenna for Quasi Elliptic Band Pass Response.

**Resource:Indian Patent Advaced Search System  Publication dated 29.05.2020**