Code No: 124CN

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2017
COMPUTER ORGANIZATION
(Computer Science and Engineering)

Time: 3 Hours   Max. Marks: 75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART-A
(25 Marks)

1.a) Define the effective address. [2]
 b) Explain about Logical and Bit Manipulation Instructions. [3]
 c) Explain about the purpose of Input-output interface. [2]
 d) Explain about the two-wire control. [3]
 e) Explain about auxiliary memory. [2]
 f) What is a bootstrap loader? Explain about the functions of bootstrap loader. [3]
 g) Explain about the purpose of Bus High Enable pin in 8086. [2]
 h) Explain about condition code flag register in 8086. [3]
 i) Explain about One-byte instruction in 8086. [2]
 j) Explain about FAR PTR and NEAR PTR assembler directive. [3]

PART-B
(50 Marks)

2. Write a program to evaluate the arithmetic statement:

$$X = A - B + C * (D * E - F)$$
$$G + H * K$$

 a) Using a general register computer with three address instructions.
 b) Using a general register computer with two address instructions. [5+5]

OR

3.a) Explain about the functions of CPU.
 b) Explain about Program Control Instructions. [5+5]

4.a) Explain about Source-initiated transfer using handshaking and Destination-initiated transfer using handshaking with a neat diagram.
 b) A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram. [5+5]

OR

5.a) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?
 b) Explain about Intel 8089 IOP. [5+5]

6. A computer uses RAM chips of 1024×1 capacity.
   a) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?
   b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [5+5]

OR

7.a) Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.

b) Explain about Virtual Memory with the implementation details. [5+5]

8.a) Explain about the register organization of 8086.

b) Explain about the concept of segmented memory with a neat diagram. Explain its advantages. [5+5]

OR

9.a) Explain about addressing modes of 8086.

b) Explain about the functions of opcode prefetch queue in an 8086 system. [5+5]

10.a) Explain about different instruction formats in 8086.

b) Write an Assembly Language program to perform one byte BCD addition. [5+5]

OR

11.a) Explain about different types of Assembler directives and operators.

b) Write an ALP program to find transpose of a 3×3 matrix. [5+5]

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