R13

Code No: 113BQ

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, December-2014
DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION
(Information Technology)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A **(25 Marks)**

1.a) Convert the hexadecimal number 2AC5.D to binary and octal. [2M]
b) What is Gray code and give its advantages. [3M]
c) What is race around condition? How it is avoided. [2M]
d) What is PLD? Give its advantages and also give the classification of PLD's. [3M]
e) Write about IEEE 754 floating point format. [2M]
f) Give the differences between RISC and CISC. [3M]
g) Describe the two control signals used for register transfer. [2M]
h) How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address? [3M]
i) What is bus arbitration? Mention the types of bus arbitration? [2M]
j) What is interrupt? Give its classification. [3M]

Part- B **(50 Marks)**

2.a) Explain about communication topologies used in multiprocessors.
b) Perform the arithmetic operation (-638) + (+785) with the decimal numbers using signed 10's complement representation for negative numbers.

OR

3.a) Briefly explain the basic functional units of a computer.
b) Using 2's complement perform $(42)_{10} - (68)_{10}$.

4.a) Find the reduced POS form of the function .
$F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$. Implement using NAND logic.
b) Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2, 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

OR

5. What is the difference between serial and parallel transfer. Using a shift register with parallel load, explain how to convert serial input data to parallel output and parallel input data to serial output.

6. Draw and explain with a flowchart multiplication of two signed magnitude fixed point numbers.

OR

7. What is the need for various addressing modes? Explain various addressing modes with example.

8.a) Discuss the concepts of virtual Memory.
b) Explain the design of hardwired control logic.

OR

9.a) Write about memory management requirements.
b) List and briefly explain applications of microprogramming.

10. Explain the following in detail:
a) Programmed I/O
b) Interrupt- initiated I/O.

OR

11.a) Describe an asynchronous data transfer using hand shaking with the help of timing diagram.
b) Explain about IOP in detail.

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