Code No: 114AF

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May-2015
DIGITAL DESIGN USING VERILOG HDL
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Write difference between tasks and functions.	[2M]
b)	Illustrate with an example Array of Instances of Primitives.	[3M]
c)	What are Tristate gates?	[2M]
d)	Mention data types used in Verilog HDL.	[3M]
e)	Write any two sequential models can be used.	[2M]
f)	Write about bidirectional gates.	[3M]
g)	What are parallel blocks?	[2M]
h)	What are time delays with switch primitives?	[3M]
i)	Draw the diagram of NAND gate using CMOS switches.	[2M]
j)	Write Verilog code using Case statement.	[3M]

PART-B **(50 Marks)**

2. Explain the following "lexical conventions" with examples.
a) White space b) strengths c) Operators [3+3+4]

OR

3.a) Write a short notes on concurrency and functional verification.
b) Explain port Declaration with an example using Verilog code. [5+5]

4.a) Classify and explain strengths and contention resolution.
b) Write Verilog code for 1 to 4 demultiplexer module by using 2 to 4 decoder? [5+5]

OR

5.a) Write Verilog module for a positive edge triggered flip flop with test bench.
b) Explain how the ALWAYS statements are used in Verilog. [5+5]

6.a) Design Verilog module Event construct for a serial data receive and test bench for the same.
b) Design a counter module and test bench to illustrate the use of WAIT. [5+5]

OR

7.a) Describe procedural continuous assignment statements assign, de assign, force and release.

b) Explain the compiles directives in detail. [5+5]

8.a) Design CMOS switch of parallel combination.

b) Explain and specify blocks of Path Delay Modeling. [5+5]

OR

9.a) Write the code for CMOS switch of parallel combination.

b) Briefly explain combinational and sequential UDPs in Verilog. [5+5]

10.a) Write the verilog code for basic functional unit of a dynamic shift register.

b) Write a short note on Design verification. [5+5]

OR

11.a) Briefly explain any one method used for sequential circuit testing.

b) Write Verilog module for 8-bit comparator with test bench. [5+5]

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