Code No: 118FH

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, April - 2018
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Define digital signal-processing system, explain it with a neat diagram.	[2]
b)	What are the mail features of DSP architecture, list important sub-blocks of it?	[3]
c)	Explain how pipelining is useful in increase the speed of DSP processor.	[2]
d)	Explain multiplier used in DSP processors to get high speed.	[3]
e)	List the architectural features to improve speed in TMS320C54XX DSP processor.	[2]
f)	List On-Chip Peripherals available in TMS320C54XX.	[3]
g)	Explain Shifter Instruction using in DSP processors.	[2]
h)	Draw the basic Architecture of ADSP 2100 label each sub block.	[3]
i)	What is the importance of external bus interfacing signals in DSP processors?	[2]
j)	Briefly explain how DMA is implemented in DSP processors.	[3]

PART B **(50 Marks)**

2.a)	Find the DFT of the sequence {1, 1, 1, 1, 2, 2, 2, 2} using radix-2 Decimation –in – Frequency FFT.	
b)	What is Compensating filter, explain with suitable examples.	[5+5]
	OR	
3.a)	What are the various number formats for signals and coefficients in DSP systems, explain with examples.	
b)	Explain A/D Conversion errors and DSP Computational errors.	[5+5]
4.a)	Explain Programmability and Program Execution in DSP processors.	
b)	List the DSP Computational Building Blocks, explain any two blocks.	[5+5]
	OR	
5.a)	Explain the function of a MAC unit and also explain how overflow and Under flow conditions can be avoided in MAC operations.	
b)	List features for external interfacing using with DSP processors, and explain.	[5+5]

6.a) Define addressing mode, explain ant four Data Addressing modes of MS320C54XX Processors.

b) What are the On-Chip Peripherals available in TMS320C54XX, explain briefly. [5+5]

OR

7.a) Explain memory management and memory space in TMS320C54XX DSP processors.

b) Explain Pipeline Operation in TMS320C54XX Processors with a diagram. [5+5]

8.a) With the help of block diagram explain functionality of ADSP-2181 high performance Processor.

b) Explain Address Arithmetic Unit and Control Unit with a diagram. [5+5]

OR

9.a) Explain different architectural features of Blackfin Processor with a diagram.

b) What are the register files, explain Hardware Processing Units? [5+5]

10.a) Describe how ADC interfaced to DSP in programmed I/O mode.

b) Explain the memory interface block diagram of TMS320C5416. [5+5]

OR

11.a) Describe Memory space organization in DSP with example.

b) Explain the process of interrupt handling by the DSP processor with a neat diagram. [5+5]

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