R15

Code No: 128FH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year II Semester Examinations, May - 2019
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	State the properties of twiddle factor.	[2]
b)	Write any two applications of DSPs	[3]
c)	What are the advantages of VLIW over Von Neuman architecture	[2]
d)	What is the purpose of Barrel Shifter in the processor	[3]
e)	What is the use of EMI?	[2]
f)	What is a hardware interrupt?	[3]
g)	What is the purpose of Core event controller in Blackfin processor?	[2]
h)	Mention the allotment of memory for Instruction SRAM, Data SRAM and scratchpad of Blackfin processor.	[3]
i)	How does cache memory increase the execution speed of the program?	[2]
j)	What is meant by Interrupt vector Table?	[3]

PART - B

(50 Marks)

2.a)	What are the basic elements of digital signal processing? Give the advantages of digital signal processing over analog signal processing.	
b)	State and prove sampling theorem.	[5+5]

OR

3.a)	What are the different sources of errors in DSP implementations? Explain.	
b)	Explain the decimation and interpolation process with an example. Also find the spectrum.	[5+5]

4.a)	With a neat diagram explain the basic architectural features of DSP processor.	
b)	Discuss in brief about the data addressing capabilities of programmable DSP devices with examples.	[5+5]

OR

5.a)	How the shifters are useful in DSP? Explain the functionality of barrel shifter?	
b)	Explain the features of external interfacing.	[6+4]

6.a)	Explain the Data Addressing modes of TMS320C54XX DSPs.	
b)	Describe in detail about the pipeline operation of TMS320C54XX processor.	[5+5]

OR

7.a)	With a neat diagram explain about the memory structure of TMS320C54XX processor.	
b)	Describe the operation of the following instructions: i) MAS *AR3- , *AR4+, B, A ii) MAC *AR1+ , *AR2- , A	[7+3]

8.a) Explain the base architecture of ADSP 2181.
b) Discuss about the basic peripherals of Blackfin processor. [5+5]

OR

9.a) Explain in detail about Blackfin processor.
b) Describe in detail the bus architecture of Blackfin processor. [5+5]

10.a) Discuss in detail about Direct Memory Access.
b) With a neat diagram explain about the interfacing of memory in a DSP processor. [5+5]

OR

11.a) Briefly explain programmed I/O.
b) What is the significance of Interrupts in DSP processors? Explain. [5+5]

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