R18

Code No: 153AN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, December - 2019

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART- A **(25 Marks)**

1.a) Given that $(292)_{10}=(1204)_b$, Determine b. [2]
b) Write a note on 'display decoders'. [2]
c) What is the difference between Latch and Flip Flop? [2]
d) What is Moore and Mealey machine? [2]
e) Draw the circuit for CMOS AND–OR Invert (AOI) logic gate. [2]
f) Add (98) and (89) in Excess-3 form. [3]
g) Realize the function $f_1 = A \oplus B \oplus C$ using two half adders: Use additional gates if necessary. [3]
h) Differentiate combinational and sequential circuits. [3]
i) List the limitations of finite – state machines. [3]
j) What are the precautions to be taken while handling CMOS logic gates? [3]

PART-B **(50 Marks)**

2.a) Find the complement of the Boolean function (AB′+CD′) (B′C+A′D) and reduce it to a minimum number of literals.
b) Determine the Canonical sum-of-products form for T(x,y,z)=x′y+z′+xyz. [5+5]

OR

3.a) Show the weights of three different four bit Self-Complementing codes whose only negative weight is -4.
b) Convert the function $f(x, y, z) = \pi(0, 3, 6, 7)$ to the other canonical form. [5+5]

4.a) Minimise the following expression using Karnaugh – map
$f(A,B,C,D) = \Sigma m(1,4,7,10, 13) + \Sigma d(5,14,15)$
b) Give the gate-level realization for 8:1 mux with active-low enable input. Show how several 8:1 muxes can be combined to make a 32-to-1 mux. [5+5]

OR

5.a) Using the tabular method, obtain the prime implicants of a four- input single-output function $f(w,x,y,z) = \Sigma m(0,2,4,5,6,7,8,9,10,11,13)$. Reduce the prime-implicant table and find the minimal cover of f.
b) Give the schematic circuit of a 2-to-4 binary decoder with an active-low enable input. Give the truth-table for the same. [5+5]

6.a) Draw the circuit diagram of a negative edge trigger J-K Flip-Flop with active high present and clear and explain its operation with the help of truth table.

b) Draw the circuit diagram of a mod-10 ripple counter and explain its operation with the aid of output state timing diagram. [5+5]

OR

7.a) Draw the circuit diagram of a RS flip flop and explain its operation with the help of truth table.

b) Design a modulo 6 up/down synchronous counter using T flip-flops and draw the circuit diagram. [5+5]

8. A sequential circuit with 2 D flip-flops, A and B; 2 inputs, x and y; and one output z specified by the following equations.

$A(t+1)=x'y+xA$

$B(t+1)=x'B+xA$

$Z=B$

a) Draw the logic diagram of the circuit

b) Derive the state table

c) Derive the state diagram. [3+3+4]

OR

9. A combinational lock circuit has two imports (x_1, x_2) and single output (Z) is to be designed such that the lock opens (z=1) whenever there is a sequence of form consecutive input changes with $x_2 = 1$. Construct the state diagram and stable table for this circuit. [10]

10.a) What is meant by Tri-state logic? Draw the circuit of Tri-state TTL logic and explain its functions.

b) Discuss current sinking, current sourcing and noise margins of a standard TTL logic gate. [5+5]

OR

11.a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation?

b) Describe CMOS driving TTL. [6+4]

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