R16

Code No: 136BF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, May - 2019

DIGITAL SYSTEM DESIGN

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) What is state reduction and what is the need for state reduction. [2]
b) Describe the capabilities and limitations of FSM. [3]
c) Write notes on RAM, its operation and its types. [2]
d) Implement the following function using a suitable decoder and an OR gate: $F(A,B) = \Sigma(0,1,2)$ [3]
e) What are SM charts and what are the important components in SM chart? [2]
f) Explain how an ASM chart differ from a software flow chart. [3]
g) Explain about struck at faults. [2]
h) Write a short note on Fault classes and Models. [3]
i) Give the limitations of fault diagnosis method for sequential circuit. [2]
j) Describe the need of functional testing methods. [3]

PART - B

(50 Marks)

2. Determine which of the machines with the following specifications is realizable with a finite number of states. If any machine is not realizable explain why.
a) A machine is to produce an output of 1whenever the number of 1's in the input sequence, starting at t=1, exceeds the number of 0's. For example if the input is 01100111, the required output is 00100011.
b) A machine with a single input line and 10 output lines numbered 0 through 9 is to be designed so that, following the nth input pulse, only one output pulse will be produced in the line whose corresponding number is equal to the nth digit of π (i.e, 3.14). [5+5]

OR

3. For the incompletely specified sequential machine given below find the minimal reduced machine which covers the given machine. [10]

PS	Next State, Output Input			
	0	1	2	3
a	--	g,-	e,1	d,-
b	a,-	d,-	--	-,0
c	c,-	-,0	--	g,1
d	e,0	--	a,-	--
e	-,1	f,-	-,1	-,1
F	-,1	e,-	a,1	-,1
G	f,-	-,1	b,-	h,-
h	c,-	--	a,0	--

4. Realize the following set of simultaneous equation using PAL, PLA and PROM. Compare these Programming Technologies. [10]

$F_1(W, X, Y, Z) = X'Y'Z+WX'Y+WYZ$
$F_2(W, X, Y, Z) = X'Y'Z'+W'XYZ+WYZ'+XYZ$
$F_3(W, X, Y, Z) = X'YZ+XYZ+WXYZ$

OR

5.a) With a neat block diagram explain in detail about binary multiplier.
b) Describe the overview of a score board controller and also explain the state graph of a score board controller. [5+5]

6. Derive an SM chart for an electronic dice game. [10]

OR

7. Describe the realization of a binary counter using one PLA and two D-FlipFlops. [10]

8. Explain how Kohavi algorithm can be used to detect multiple faults in a two level network with an example. [10]

OR

9.a) Explain in detail about PODEM.
b) Describe the transition test counting with an example. [5+5]

10.a) Give the detailed procedure of circuit test approach of sequential circuits.
b) Explain the procedure how to find fault detection and location in sequential circuits. [5+5]

OR

11. Explain in detail about state identification and fault detection experiment. [10]

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