

R16

Code No: 134CF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, April - 2018

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, MCT)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 Marks)

- 1.a) What is self complementing code? Give example. [2]
- b) State and Prove Demorgan's theorem. [3]
- c) What are Hazards? List their types. [2]
- d) Design 2×1 Multiplexer with neat logic diagram. [3]
- e) Write the characteristic table of JK Flip flop. [2]
- f) Draw the logic diagram of Master-Slave D flip flop. Use NAND gates. [3]
- g) What is switch tail ring counter? [2]
- h) What is a Ring Counter? What are applications of Ring counters? [3]
- i) What is an ASM Block? [2]
- j) Define merger graph of n-state machine M. [3]

PART-B

(50 Marks)

- 2.a) i) Convert the given Octal number $(2564.603)_8$ to Hexadecimal Number.
ii) Given that $(81)_{10} = (100)_b$, Find the value of b.
b) Encode data bits 1101 into 7 bit even parity Hamming Code. [5+5]
- OR**
- 3.a) Prove that $AB'C + B + BD' + ABD' + A'C = B + C$.
b) Simplify the following expression $F = AB' + ABD + ABD' + A'C'D' + A'BC'$ and implement with NAND gates. [5+5]
- 4.a) Design a code converter that converts BCD messages into Excess-3 code. The converter has four input lines carrying signals labeled w, x, y and z and four output lines carrying signals f1, f2, f3, and f4.
b) Simplify the following Boolean expression using K-map and implement them with NOR logic gates
 $F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$ [5+5]
- OR**
- 5.a) Design and explain 3 to 8 decoder with necessary truth table and logic diagram.
b) Write short notes on Hazards and Hazard free relations. [5+5]