

Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**B.Tech II Year I Semester Examinations, November - 2015****SWITCHING THEORY AND LOGIC DESIGN****(Common to ECE, EIE, ETM)****Time: 3 Hours****Max. Marks: 75****Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART- A**(25 Marks)**

- 1.a) Convert $(FFF)_{16} = (\quad)_{10}$. [2M]
- b) Draw the 1-bit comparator diagram with logic diagram. [3M]
- c) Implement 1-bit Full adder using gates. [2M]
- d) Implement one bit half subtractor using Gates. [3M]
- e) Draw the excitation table of JK Flip Flop. [2M]
- f) Write the excitation table of D flip flop. [3M]
- g) Define state diagram. [2M]
- h) Define FSM. [3M]
- i) How are asynchronous sequential machine characterized? [2M]
- j) What is the difference between Mealy and Moore Models? [3M]

PART-B**(50 Marks)**

- 2.a) Solve the following:
 - i) $(27.125)_{10} = (\quad)_8$
 - ii) $(10.6875)_{10} = (\quad)_2$
 - iii) $(237.75)_8 = (\quad)_{10}$
- b) Obtain the complement of the following Boolean expressions
 - i) $A'B + A'BC' + A'BCD + A'BC'D'E$
 - ii) $A + B + A'B'C$. [5+5]

OR

- 3.a) Encode the decimal numbers into:
 - i) $(56)_{10} = (\quad)$ Gray code
 - ii) $(20.305)_{10} = (\quad)$ Excess-3 code
 - iii) $(32.89)_{10} = (\quad)$ BCD code
- b) Realize the following logic function using only NAND gates
 $f(a,b,c,d) = \Sigma (0,2,4,6,9,11,13,15)$. [5+5]

- 4.a) Minimize the following function using K-map.
 $f(A,B,C,D) = \Sigma_m (0, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 13)$
- b) Minimize the following expression using K-map and realize using NOR gates.
 $f(A,B,C,D) = \prod M (1, 2, 3, 8, 9, 10, 11, 15)$. [5+5]

OR

- 5.a) Determine the prime implicants of the function.
 $f(W,X,Y,Z) = \Sigma (1,4,6,7,8,9,10,11,15)$. Also minimize the logic function using Tabulation method.
- b) Implement the following logic function using 16:1 Multiplexer and 8:1 Multiplexer.
 $f(a,b,c,d) = \Sigma (0,3,4,8,9,15)$. [5+5]

- 6.a) Explain the techniques used to eliminate racing condition in JK flip flops.
b) Design a S-R latch using 2-input NAND gates. [5+5]

OR

- 7.a) Convert a clocked S-R flip flop to a T-flip flop.
b) Explain the design of a clocked Flip-Flop. [5+5]

- 8.a) Design a 4-bit binary UP/DOWN ripple counter.
b) What are the different types of registers? Explain the Serial Input Parallel Output Shift register. [5+5]

OR

- 9.a) Explain the operation of RS-clocked flip-flop with logic diagram. Show the relevant waveforms.
b) Design a mod-10 Ripple counter using T flip flops and explain its operation. [5+5]

- 10.a) Discuss about completely and incompletely specified sequential machines.
b) What are State Machine charts? What are the principal components of State Machine chart? [5+5]

OR

- 11.a) Implement a weighing machine with the help of SM Chart.
b) Draw the typical flow chart, State Machine chart and state graph diagrams. [5+5]

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