Code No: 154AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, November/December - 2020
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Explain various number systems and codes and their conversion with examples for each.
b) Simplify the following Boolean expressions to a minimum number of literals:
i) ABC+A'B+ABC' (ii) xy + x(wz+wz') [9+6]

2.a) Express the following numbers in decimal : $(10110.0101)_2$, $(16.5)_{16}$, $(26.24)_8$.
b) Demonstrate by means of truth tables the Boolean Associative law and distributive law. Simplify the Boolean expression to minimum number of literals: (A+B)' (A'+B'). [8+7]

3.a) Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates.
$F(A,B,C,D) = \sum 0,2,4,5,6,7,8,10,13,15)$
b) Show that the dual of the exclusive OR is also its compliment. [9+6]

4.a) Draw the multiple level NAND circuit for the following expression:
$(AB'+CD')E + BC(A+B)$
b) Construct a 4-bit BCD adder-substractor circuit using BCD adder and 9's complemented. [7+8]

5.a) Design 4-bit shift register using D flip-flops.
b) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6, use JK flip-flops. [6+9]

6.a) Draw the circuit diagram of a 4-bit binary counter with parallel load and explain its working with its function table.
b) Design a 4 bit synchronous counter with D flip - flops and explain its working. [8+7]

7.a) Explain the working of R-2R ladder DAC with neat circuit diagram and mention it's limitations.
b) Draw and explain the working principle of flash type ADC. [8+7]

8.a) Explain the functions and applications of PLAs in memory addressing and implement the following two Boolean functions with a PLA:
$F_1(A, B, C) = \sum (0, 1, 3, 5)$ and $F_2(A, B, C) = \sum (1, 2, 4, 7)$
b) What are sequential programmable devices? Draw the sequential programmable logic for a basic microcell logic. [8+7]

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