R13

Code No: 114AE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2016
ELECTRONIC CIRCUITS
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **[25 Marks]**

1.a) Why is a CE amplifier widely used? List down its main limitations. [2]
b) What are the main advantages of negative feedback? [3]
c) What is base-spreading resistance? [2]
d) What is the bypass capacitor and why it is connected in CE amplifier? [3]
e) Name two different methods of pulse triggering. [2]
f) What are the applications of voltage comparator? [3]
g) What are the advantages of class-B operation? [2]
h) What is high pass circuit? [3]
i) Explain piece wise linear diode characteristics. [2]
j) What are the transistor switching times? [3]

PART-B **[50 Marks]**

2.a) Derive the equations for: i) Voltage gain ii) Current gain iii) Input Resistance iv) Output resistance for BJT CE configuration using h-parameters model.
b) A CE amplifier is drawn by a voltage source of internal resistance R_S = 800 ohms and load impedance is a resistance R_L = 1000 ohms. The h-parameters are h_{ie} = 1.0 K ohms, $h_{re} = 2 \times 10^{-4}$, h_{fe} = 50 and h_{oe} = 25 μ A/V. Compute A_I, R_I, A_V, R_o using approximate analysis. [5+5]

OR

3.a) Show that bandwidth increases in negative feedback amplifiers.
b) An amplifier has an input resistance of 200 K ohms, with a certain negative feedback introduced in the above amplifier the input resistance is found to be 20 M ohms and overall gain is found to be 1000. Calculate the loop gain and feedback factor. [5+5]

4.a) Derive the equation for the lower 3dB frequency of CE configuration due to emitter bypass capacitor.
b) Given the following transistor measurements made at I_C=5mA and V_{CE}=5V and at room temperature. h_{ie}=600ohms, h_{fe}=100, $C_{b'c}$=3PF and A_i=10 at 10MHZ. Find f_β, f_T, $c_{b'e}$, $r_{b'e}$ and $r_{bb'}$ of hybrid equivalent circuit in CE configuration. [5+5]

OR

5. Derive all components in the Hybrid-π model in terms of h parameters in CE configuration. [10]

6.a) Design a collector coupled monostable multivibrator with the following specifications. V_{cc} = +12V, V_{bb} = -6V, h_{FEmin} = 20, V_{EBO} = 5V, I_c = 20mA. Transistors are of silicon npn type. Output pulse width = 200μsec.

b) With the help of a neat circuit diagram, explain the operation of a astable multivibrator. [5+5]

OR

7.a) With help of a neat circuit diagram and waveforms explain the operation of An Emitter coupled clipper.

b) With help of a neat circuit diagram and waveforms explain the working of a negative clamping circuit. [5+5]

8.a) Derive the expression for maximum conversion efficiency for a simple series fed Class A power amplifier.

b) List out the advantages of complementary symmetry configuration over push pull configuration. [5+5]

OR

9.a) Derive the expression for the percentage tilt of the output of high pass circuit with large time constant excited by a symmetrical square wave with zero average value.

b) 1 kHz square wave output from an amplifier has rise time t_r = 350ns and tilt is 5%. Determine the upper and lower 3-db frequencies. [5+5]

10 a) Explain the operation of transistor switch in saturation.

b) For a common emitter amplifier, V_{cc} = 15V, R_c = 1.5kΩ and I_B = 0.3 mA.
i) Determine the value of $h_{FE(min)}$ for saturation to occur.
ii) If R_c is changed to 500 Ω will the transistor be saturated. [5+5]

OR

11.a) Explain in detail about storage and transition times relating to diode switching times.

b) Discuss in detail about transistor switching times. [5+5]

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