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	15		15AH				R13	Pé					
					LOGICAL UNI inations, Novem								
				IC APPI	LICATIONS								
		Time: 3 hou			ectronics Engineer		Iax. Marks: 75						
1:			question paper co			<u> </u>	1 4;	· • • • • • • • • • • • • • • • • • • •					
,	Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.												
		10 H			RT - A	m.	[; <u>;</u> ,						
''		; ··	: ''	: '' PA	RT - A	* ***.*	(25 Marks)	; '					
		1 -) F1	-: ''T -4-1''	. 4 41	d . d								
6	15	b) Disc c) List d) List e) Wha	the features of 74 the non-ideal DC t is frequency sta	uffer amplifier in 1 OP-ÄMP, characteristics ob bility? Explain in	s different from an in it	PE	[2] [3] [2]	PE					
5	, et	appl i) How	cations of PLL. many resistors a	re required in a 1	Timer?	esistor DAC? WI	[3]	PÉ.					
S		F.G.	P6	PA	RT - B	PE		FE					
			pare the TTL and gn a TTL 2-state		explain its opera	tion.	[4+6]						
**		3.a);Wha	t is interfacing? I	Explain the opera	OR ation of TTL drivi	ing CMQS:		PE					
:	1.5	b) Expl	ain the operation	of the TTL oper	collector outputs	s. !:	[5+5]	i ''					
		appl	ications of instrui	nentation amplif	What are the feater.								
• •		√b) Deri ;''':'''	ve input resistanc	e for inverting a	mplifier with feed OR []:	dback arrangeme	ent. [4+6]	FE,					
· j	· ·	b) In a	n AC inverting	amplifier circu	It using an op-amplit R_{in} =50 Ω , C_{i} =the Bandwidth of	p. = 0.1μF, R ₁ =10	i i: 00ΚΩ, R=1ΚΩ, [4+6]	i 1i					
		r, C	P6	P6°	P6	P6	P6	P6					

	Ł				2		as.					
à	Design a first order active high pass filter with cutoff frequency of 2KHz with op-amp. Why this is called Active filter? Design a Triangular wave generator with f ₀ = 1.5 KHz and V ₀ (PP) = 5V. [5+5] Design a 555 timer monostable multivibrator applications in pulse stretching. Design a 555 timer circuit whose output frequency is 2KHz when the trigger input signal frequency is 4KHz. OR											
:												
÷	9.a) Explain the operation of frequency multiplier using PLL. Define Lock-in range, Capture range and Pull-in time in PLL system. 10.a) Compare the dual slope ADC with successive approximation ADC. b) Explain the operation of R-2R ladder DAC with the help of neat diagrams. [4+6]											
	Jł.a) Expla	in the operation of are the merits an	of flash ADC usi d demetits of co	OR ng relevant diago unter type::ADC?	rams. Explain	: <u>[</u> [6+4]						
	P6	P6		O00	P6	P6	P6					
	P6	P6	P6	P6	PG	P6	P6					
	PG	P6	P6	P6	P6	P6	P6					
	P6	P6	P6	P6	P6	P6	P6					
	P6	P6	P6	P6	P6	P6	P6					