Code No: 114DT

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2015
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, BME)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define Binary coded decimal code. [2M]
b) Draw the logic diagram of NAND gate and explain. [3M]
c) Define combinational circuit. [2M]
d) Write short notes on Multiplexers. [3M]
e) Define Flip Flop. [2M]
f) What is the difference between sequential and combinational circuits? [3M]
g) Define state diagram. [2M]
h) Write short notes on ripple counter. [3M]
i) Define ASM Chart. [2M]
j) Explain briefly about partition techniques. [3M]

PART – B

(50 Marks)

2.a) Convert the number $(1222)_3$ into decimal and Hexadecimal number system.
b) Add and multiply the numbers $(23)_5$ and $(345)_6$ without converting to decimal.
c) Consider a function 'F'. Show that F.F'=0 and F+F'=1. [3+4+3]

OR

3.a) Convert the number $(4413)_5$ into decimal and Hexadecimal number system.
b) Find the 9's complement of the numbers 12345678, 87654321.
c) Express the function B'D+A'D+BD in sum of minterms and product of maxterms. [3+3+4]

4.a) Simplify the Boolean function F(A,B,C,D) = Σ(4,5,6,8,15) using four variable maps.
b) Simplify the expression BD+BCD'+AB'C'D' and implement them with two level NAND gate circuit.
c) Design a three input majority function such that the output is 1 if the input has even number of 1's otherwise the output is 0. [4+3+3]

OR

5.a) Simplify the Boolean function F(A,B,C,D) = Σ(0,2,3,5,7,8,10,11) by first finding the essential prime implicants.
b) Draw a logic diagram using two input NOR gates to implement the expression (AB+A'B')(CD'+C'D)
c) Design a combinational circuit with three inputs and one output. The output is equal to logic-1 when the binary value of the input is less than 4 otherwise the output is logic-0. [3+3+4]

6.a) Draw the structure of D-Flip Flop and write its truth table.
b) Write short notes on Binary Cell.
c) Design T Flip Flop using any other Flip Flop. [3+4+3]

OR

7.a) Draw the structure of T-Flip Flop and write its truth table.
b) What are the fundamentals of the Sequential Machine Operation?
c) Design JK Flip Flop using any other Flip Flop. [3+3+4]

8.a) What is a synchronous sequential circuit? Explain its analysis.
b) Explain in detail about shift Register.
c) How many Flip Flops will be complemented in a 10 bit binary ripple counter to reach the next count after counting 1111110011? [3+4+3]

OR

9.a) Write short notes on synchronous sequential finite state machines.
b) Explain the design of ring counter using shift registers.
c) Draw the logic diagram of a 4 bit binary ripple counter using flip flops that trigger on negative edge transition. [3+4+3]

10.a) Explain the capabilities of finite state machine.
b) Explain the concept of minimal cover table.
c) Derive the state table for the ASM chart of data processor subsystem for the binary multiplier [3+3+4]

OR

11.a) Explain in detail about Mealy and Moore model.
b) Explain about the system design using data path and control sub systems.
c) Design the control circuit of binary multiplier using D Flip Flops and decoder. [4+3+3]

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