ACE Engineering College
(with a Difference in Excellence)
An AUTONOMOUS Institution

Question Paper Code: CS304PC

ACE-R20

Semester Supplementary Examination
II B. Tech- I Semester- SEPTEMBER-2022
COMPUTER ORGANIZATION and ARCHITECTURE
(Common to CSE,CSM,CSD)

Time: 3 Hours **Max. Marks: 70**

H. T. No										

Answer any 5 Questions out of 8 Questions from the following

Q.No	Question	M
1. a)	Demonstrate the operations and implementation of the arithmetic logic shift unit.	7
b)	Name the memory reference instructions and interpret each instruction.	7
2. a)	List out and discuss the logic micro operations and shift micro operations.	7
b)	Define interrupt. Why do interrupts occur? Draw the flowchart for instruction cycle.	7
3. a)	Show the block diagram of control memory and the associated hardware needed for selecting the next microinstruction address.	7
b)	Assess the procedure for the evaluation of arithmetic expressions.	7
4. a)	Interpret any seven addressing modes with the syntax and examples.	7
b)	Differentiate between CISC and RISC processors.	7
5. a)	Illustrate the procedure for Booth algorithm to perform multiplication.	7
b)	Outline the representation of fixed-point and floating-point numbers.	7
6. a)	Analyze the possible modes of data transfer to and from peripherals.	7
b)	Define associative memory. Show the block diagram of associative memory and representation of associative memory of m word, n cells per word.	7
7. a)	Explain the usage of strobe and handshaking methods for aschronous data transfer.	7
b)	Discuss the mechanism related to mapping procedures of cache memory	7
8. a)	Outline the architecture of 8086 processor and summarize the register organization of 8086 processor.	7
b)	Explain with a neat diagram Instruction Pipeline.	7